Document Title

16M DDR SYNCHRONOUS SRAM

Revision History

Rev No.	History	Draft Data	Remark
Rev. 0.0	Initial document.	Feb. 2003	Advance
Rev. 0.1	Remove K7D163688B	Jun. 2003	Advance
Rev. 0.2	Change AC CHARACTERISTICS -Data Setup time -33 : 0.25 -> 0.3 -Data Hold time -33 : 0.25 -> 0.3 -Remove : t_{QTRK}, t_{CXCV} -Add : t_{CXCH},t_{CXCL},t_{CHQV},t_{CLQV},t_{CHQX},t_{CLQX},t_{CLQZ},t_{CHLZ} Change RECOMMENDED DC OPERATING CONDITIONS -Input Reference Voltage (Max) : 1.0 -> 0.95 Change DC CHARACTERISTICS - Fill up the blank(TBD) - Change I_{SB1} : 150 -> 100	Sep. 2003	Advance
Rev. 0.3	Change PACKAGE PIN CONFIGURATIONS - Remove the number at DQ pins	Oct. 2003	Advance

FEATURES

- 1Mx18 Organizations.
- 1.8V V_{DD}/1.5V V_{DDQ}.(1.9V max V_{DDQ})
- HSTL Input and Outputs.
- Single Differential HSTL Clock.
- Synchronous Pipeline Mode of Operation with Self-Timed Late Write.
- Free Running Active High and Active Low Echo Clock Output Pin.
- Asynchronous Output Enable.
- Registered Addresses, Burst Control and Data Inputs.
- Registered Outputs.
- Double and Single Data Rate Burst Read and Write.
- Burst Count Controllable With Max Burst Length of 4
- Interleved and Linear Burst mode support
- Bypass Operation Support
- Programmable Impedance Output Drivers.
- JTAG Boundary Scan (subset of IEEE std. 1149.1)
- 153(9x17) Pin Ball Grid Array Package(14mmx22mm)

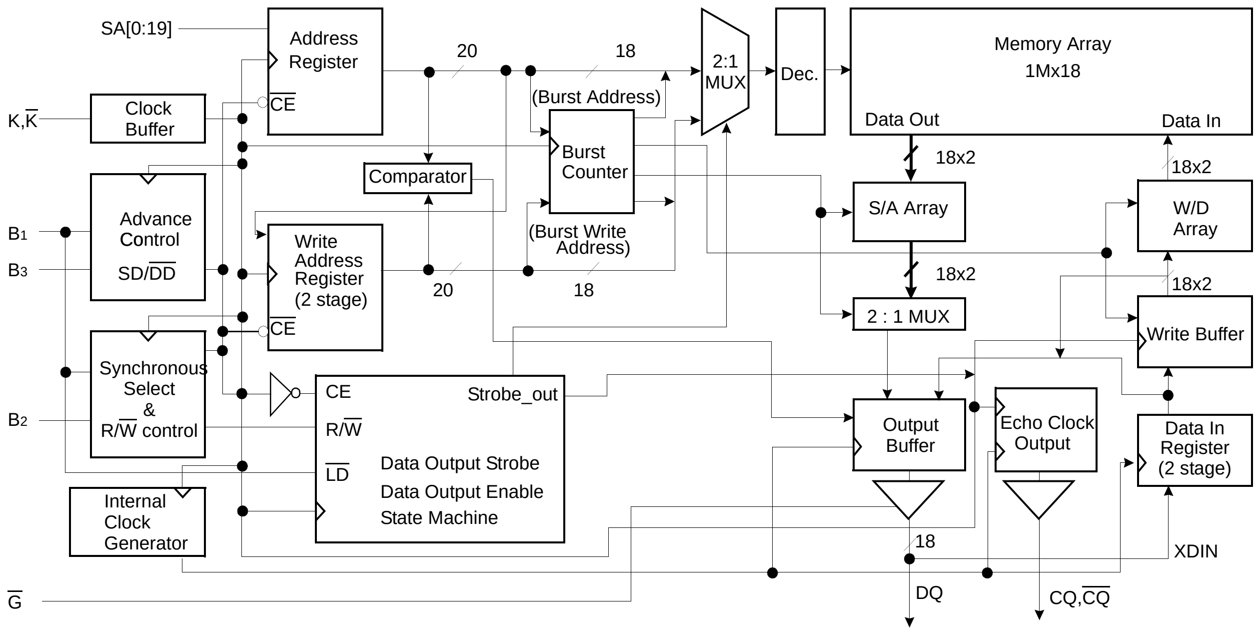
GENERAL DESCRIPTION

The K7D161888B are 18,874,368 bit Synchronous Pipeline Burst Mode SRAM devices. They are organized as 1,048,576 words by 18 bits for K7D161888B, fabricated using Samsung's advanced CMOS technology.
Single differential HSTL level clock, K and $\overline{K}$ are used to initiate the read/write operation and all internal operations are self-timed. At the rising edge of K clock, all addresses and burst control inputs are registered internally. Data inputs are registered one cycle after write addresses are asserted(Late Write), at the rising edge of K clock for single data rate (SDR) write operations and at rising and falling edge of K clock for a double data rate (DDR) write operations.
Data outputs are updated from output registers off the rising edges of K clock for SDR read operations, and off the rising and falling edges of K clock for DDR read operations. Free running echo clocks are supported which are representive of data output access time for all SDR and DDR operations.
The chip is operated with a single +1.8V power supply and is compatible with Extended HSTL input and output. The package is 9x17(153) Ball Grid Array balls on a 1.27mm pitch.

ORDERING INFORMATION

Part Number	Organization	Maximum Frequency
K7D161888B-HC37	1Mx18	370MHz
K7D161888B-HC33		333MHz
K7D161888B-HC30		300MHz
K7D161888B-HC25		250MHz

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

Pin Name	Pin Description	Pin Name	Pin Description
K, $\overline{K}$	Differential Clocks	ZQ	Output Driver Impedance Control Input
SA	Synchronous Address Input	TCK	JTAG Test Clock
SA_0, SA_1	Synchronous Burst Address Input (SA0 = LSB)	TMS	JTAG Test Mode Select
DQ	Synchronous Data I/O	TDI	JTAG Test Data Input
CQ, $\overline{CQ}$	Differential Output Echo Clocks	TDO	JTAG Test Data Output
B_1	Load External Address	V_{REF}	HSTL Input Reference Voltage
B_2	Burst R/$\overline{W}$ Enable	V_{DD}	Power Supply
B_3	Single/Double Data Selection	V_{DDQ}	Output Power Supply
$\overline{G}$	Asynchronous Output Enable	V_{SS}	GND
$\overline{LBO}$	Linear Burst Order	NC	No Connection

PACKAGE PIN CONFIGURATIONS(TOP VIEW)

K7D161888B(1Mx18)

	1	2	3	4	5	6	7	8	9
A	VSS	VDDQ	SA	SA	ZQ	SA	SA	VDDQ	VSS
B	NC	DQ	SA	VSS	B1	VSS	SA	NC	DQ
C	VSS	VDDQ	SA	SA	$\overline{\text{G}}$	SA	SA	VDDQ	VSS
D	DQ	NC	SA	VSS	VDD	VSS	SA	DQ	NC
E	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
F	NC	CQ1	NC	VDD	VDD	VDD	DQ	NC	DQ
G	VSS	VDDQ	VSS	VSS	K	VSS	VSS	VDDQ	VSS
H	DQ	NC	DQ	VDD	$\overline{\text{K}}$	VDD	NC	DQ	NC
J	VSS	VDDQ	VSS	VDD	VDD	VDD	VSS	VDDQ	VSS
K	NC	DQ	NC	VSS	B2	VSS	DQ	NC	DQ
L	VSS	VDDQ	VSS	$\overline{\text{LBO}}$	B3	MODE	VSS	VDDQ	VSS
M	DQ	NC	DQ	VDD	VDD	VDD	NC	$\overline{\text{CQ1}}$	NC
N	VSS	VDDQ	VSS	VDD	VREF	VDD	VSS	VDDQ	VSS
P	NC	DQ	SA	VSS	VDD	VSS	SA	NC	DQ
R	VSS	VDDQ	VDD	SA	SA1	SA	VDD	VDDQ	VSS
T	DQ	NC	SA	VSS	SA0	VSS	SA	DQ	NC
U	VSS	VDDQ	TMS	TDI	TCK	TDO	NC	VDDQ	VSS

* Mode Pin(6L)is a internally NC.

Read Operation(Single and Double)

During SDR read operations, addresses and controls are registered at the first rising edge of K clock and then the internal array is read between first and second rising edges of K clock. Data outputs are updated from output registers off the second rising edge of K clock. During DDR read operations, addresses and controls are registered at the first rising edge of K clock, and then the internal array is read twice between first and second rising edges of K clock. Data outputs are updated from output registers sequentially by burst order off the second rising and falling edge of K clock.
Interleave and linear burst operation is controlled by $\overline{\text{LBO}}$ pin and the burst count is controllable with the maximum burst length of 4. To avoid data contention,at least one NOP operations are required between the last read and the first write operation.

Write Operation(Late Write)

During SDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered at the following rising edge of K clock. During DDR write operations, addresses and controls are registered at the first rising edge of K clock and data inputs are registered twice at the following rising and falling edge of K clock. Write addresses and data inputs are stored in the data in registers until the next write operation, and only at the next write opeation are data inputs fully written into SRAM array.

Echo clock operation

Free running type of Echo clocks are generated from K clock regardless of read, write and NOP operations. They will stop operation only when K clock is in the stop mode.
Echo clocks are designed to represent data output access time and this allows the echo clocks to be used as reference to capture data outputs outputs.

Bypass Read Operation

Bypass read operation occurs when the last write operation is followed by a read operation where write and read addresses are identical. For this case, data outputs are from the data in registers instead of SRAM array.

Programmable Impedance Output Driver

The data output and echo clock driver impedance are adjusted by an external resistor, RQ, connected between ZQ pin and V_{SS}, and are equal to RQ/5. For example, 250Ω resistor will give an output impedance of 50Ω. Output driver impedance tolerance is 15% by test(10% by design) and is periodically readjusted to reflect the changes in supply voltage and temperature. Impedance updates occur early in cycles that do not activate the outputs, such as deselect cycles. They may also occur in cycles initiated with $\overline{\text{G}}$ high. In all cases impedance updates are transparent to the user and do not produce access time "push-outs" or other anomalous behavior in the SRAM. Impedance updates occur no more often than every 32 clock cycles. Clock cycles are counted whether the SRAM is selected or not and proceed regardless of the type of cycle being executed. Therefore, the user can be assured that after 33 continuous read cycles have occurred, an impedance update will occur the next time $\overline{\text{G}}$ are high at a rising edge of the K clock. There are no power up requirements for the SRAM. However, to guarantee optimum output driver impedance after power up, the SRAM needs 1024 non-read cycles.

Power-Up/Power-Down Supply Voltage Sequencing

The following power-up supply voltage application is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF}, then V_{IN}. V_{DD} and V_{DDQ} can be applied simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-up. The following power-down supply voltage removal sequence is recommended: V_{IN}, V_{REF}, V_{DDQ}, V_{DD}, V_{SS}. V_{DD} and V_{DDQ} can be removed simultaneously, as long as V_{DDQ} does not exceed V_{DD} by more than 0.5V during power-down.

TRUTH TABLE

K	$\overline{G}$	B1	B2	B3	DQ	Operation
L	X	X	X	X	Hi-Z	Clock Stop
↑	X	H	L	X	Hi-Z	No Operation, Pipeline High-Z
↑	L	L	H	H	DOUT	Load Address, Single Read
↑	L	L	H	L	DOUT	Load Address, Double Read
↑	X	L	L	H	DIN	Load Address, Single Write
↑	X	L	L	L	DIN	Load Address, Double Write
↑	X	H	H	X	B	Increment Address, Continue

NOTE : - B(Both) is DIN in write cycle and DOUT in read cycle. Byte write function is not supported. X means "Don't Care".
- K & $\overline{K}$ are complementary.

BURST SEQUENCE TABLE

4 Burst Operation for Interleaved Burst ($\overline{LBO}$ = VDDQ)

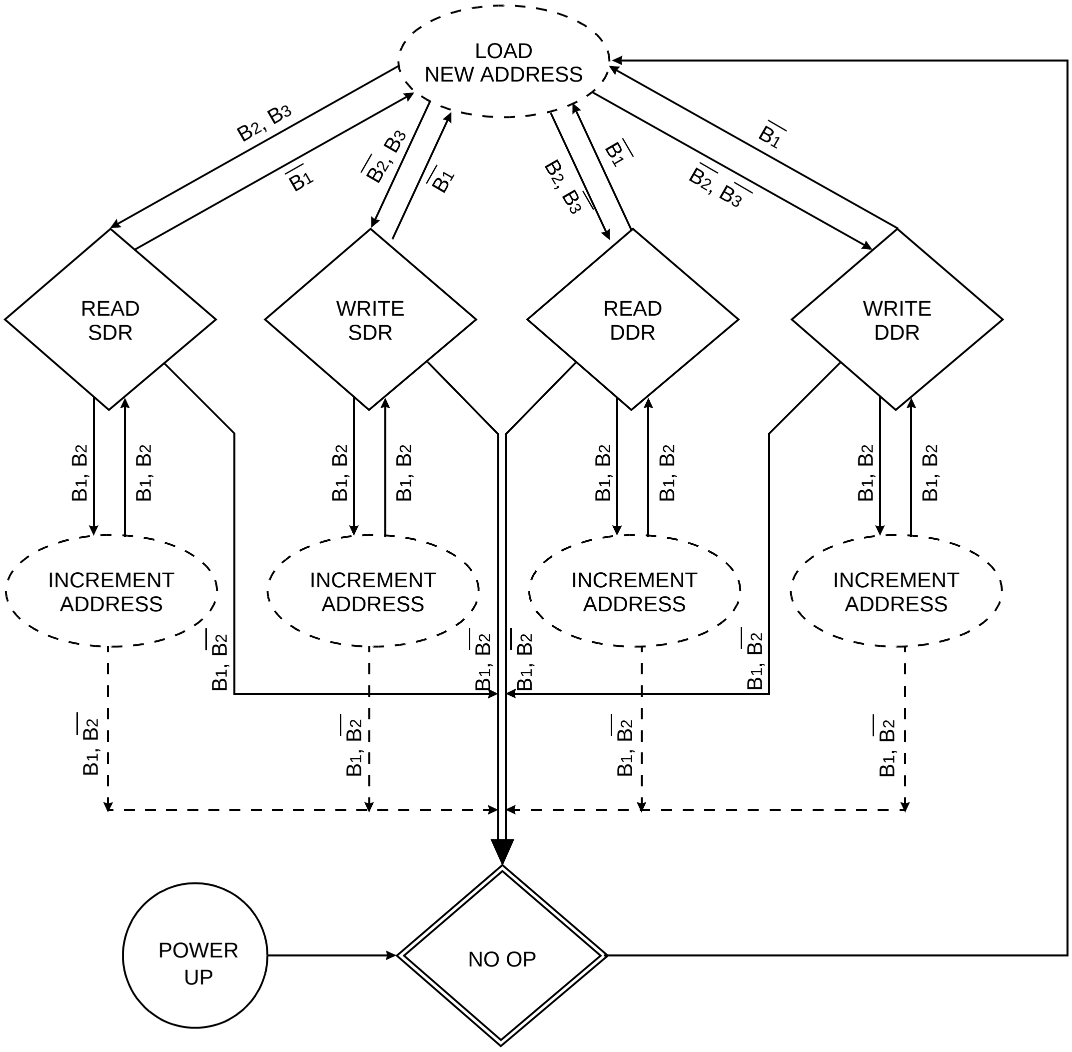
Interleaved Burst	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	0	0	1	1	1	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	1	0	0	1	0	0

NOTE : - For Interleave Burst $\overline{LBO}$ = VDDQ is recommended. If $\overline{LBO}$ = VDD, it must not exceed 1.9V.

4 Burst Operation for Linear Burst ($\overline{LBO}$ = Vss)

Linear Burst Mode	Case 1		Case 2		Case 3		Case 4	
	A1	A0	A1	A0	A1	A0	A1	A0
First Address	0	0	0	1	1	0	1	1
	0	1	1	0	1	1	0	0
↓	1	0	1	1	0	0	0	1
Fourth Address	1	1	0	0	0	1	1	0

BUS CYCLE STATE DIAGRAM



NOTE :

1. State transitions ; $\overline{B_1}$ =(Load Address), B_1=(Increment Address, Continue)
   B_2 =(Read), $\overline{B_2}$ =(Write)
   B_3 =(Single Data Rate), $\overline{B_3}$ =(Double Data Rate)

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Core Supply Voltage Relative to V_{SS}	V_{DD}	-0.5 to 2.3	V
Output Supply Voltage Relative to V_{SS}	V_{DDQ}	-0.5 to 2.3	V
Voltage on any pin Relative to V_{SS}	V_{IN}	-0.5 to V_{DDQ}+0.5	V
Output Short-Circuit Current(per I/O)	I_{OUT}	25	mA
Storage Temperature	T_{STR}	-55 to 125	°C

NOTE : Power Dissipation Capability will be dependent upon package characteristics and use environment. See enclosed thermal impedance data. Stresses greater than those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Core Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Output Power Supply Voltage	V_{DDQ}	1.4	1.5	1.9	V	
Input High Level Voltage	V_{IH}	V_{REF}+0.1	-	V_{DDQ}+0.3	V	1, 2
Input Low Level Voltage	V_{IL}	-0.3	-	V_{REF}-0.1	V	1, 3
Input Reference Voltage	V_{REF}	0.68	0.75	0.95	V	

NOTE :1. These are DC test criteria. DC design criteria is $V_{REF}\pm$50mV. The AC V_{IH}/V_{IL} levels are defined separately for measuring timing parameters.
2. V_{IH} (Max)DC=V_{DDQ}+0.3, V_{IH} (Max)AC=2.6V (2.1V for DQs) (pulse width $\leq$ 20% of cycle time).
3. V_{IL} (Min)DC=-0.3V, V_{IL} (Min)AC=-1.0V (-0.5V for DQs) (pulse width $\leq$ 20% of cycle time).

DC CHARACTERISTICS

Parameter	Symbol	Min	Max	Unit	Note
Average Power Supply Operating Current (Cycle time = t_{KHKH} min)	I_{DD37} I_{DD33} I_{DD30} I_{DD25}	-	500 450 400 350	mA	1,2
Stop Clock Standby Current (V_{IN}=V_{DD}-0.2V or 0.2V fixed, K=Low, $\overline{K}$=High)	I_{SB1}	-	100	mA	1
Input Leakage Current (V_{IN}=V_{SS} or V_{DDQ})	I_{LI}	-1	1	µA	
Output Leakage Current (V_{OUT}=V_{SS} or V_{DDQ})	I_{LO}	-1	1	µA	
Output High Voltage(Programmable Impedance Mode)	V_{OH1}	V_{DDQ}/2	V_{DDQ}	V	3
Output Low Voltage(Programmable Impedance Mode)	V_{OL1}	V_{SS}	V_{DDQ}/2	V	4
Output High Voltage(I_{OH}=-0.1mA)	V_{OH2}	V_{DDQ}-0.2	V_{DDQ}	V	5
Output Low Voltage(I_{OL}=0.1mA)	V_{OL2}	V_{SS}	0.2	V	5

NOTE :1. Minimum cycle. I_{OUT}=0mA.
2. 50% read cycles.
3. $|I_{OH}|=(V_{DDQ}/2)/(RQ/5)\pm15\%$ @$V_{OH}=V_{DDQ}/2$ for $175\Omega \leq RQ \leq 350\Omega$.
4. $|I_{OL}|=(V_{DDQ}/2)/(RQ/5)\pm15\%$ @$V_{OL}=V_{DDQ}/2$ for $175\Omega \leq RQ \leq 350\Omega$.
5. Minimum Impedance Mode when ZQ pin is connected to V_{SS}.

PIN CAPACITANCE

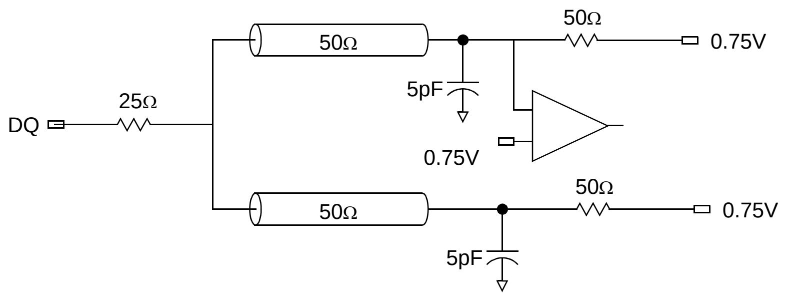
Parameter	Symbol	Test Condition	TYP	Max	Unit
Input Capacitance	C_{IN}	V_{IN}=0V	-	4	pF
Data Output Capacitance	C_{OUT}	V_{OUT}=0V	-	5	pF

NOTE : Periodically sampled and not 100% tested.(T_A=25°C, f=1MHz)

AC TEST CONDITIONS(T_A=0 to 70°C, V_{DD}=1.7 - 1.9V, V_{DDQ}=1.5V)

Parameter	Symbol	Value	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.25/0.25	V	-
Input Reference Level	V_{REF}	0.75	V	-
Input Rise/Fall Time	T_R/T_F	0.5/0.5	ns	-
Output Timing Reference Level		0.75	V	-
Clock Input Timing Reference Level		Cross Point	V	-
Output Load	See Below			-

AC TEST OUTPUT LOAD

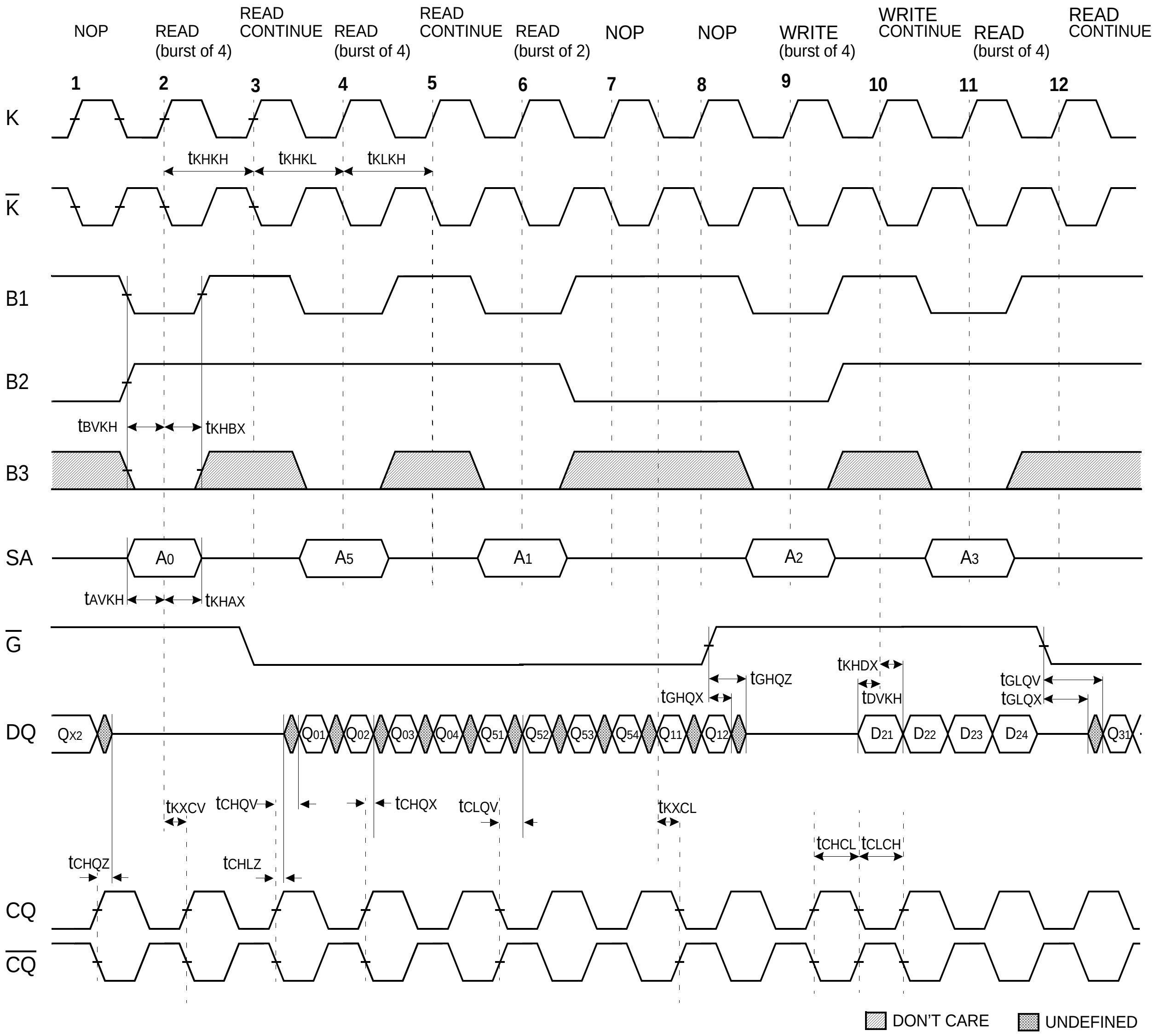


AC TIMING CHARACTERISTICS

PARAMETER	SYMBOL	-37		-33		-30		-25		UNITS	NOTES
		Min	Max	Min	Max	Min	Max	Min	Max		
Clock											
Clock Cycle Time	t_{KHKH}	2.7	-	3.0	-	3.3	-	4.0	-	ns	1
Clock High Pulse Width	t_{KHKL}	1.3	-	1.3	-	1.5	-	1.7	-	ns	
Clock Low Pulse Width	t_{KLKH}	1.3	-	1.3	-	1.5	-	1.7	-	ns	
Setup Times											
Address Setup Time	t_{AVKH}	0.4	-	0.4	-	0.4	-	0.5	-	ns	
Control(B1,B2,B3) Setup Time	t_{BVKH}	0.4	-	0.4	-	0.4	-	0.5	-	ns	
Data Setup Time	t_{DVKX}	0.25	-	0.3	-	0.3	-	0.4	-	ns	2
Hold Times											
Address Hold Time	t_{KHAX}	0.4	-	0.4	-	0.4	-	0.5	-	ns	
Control(B1,B2,B3) Hold Time	t_{KHBX}	0.4	-	0.4	-	0.4	-	0.5	-	ns	
Data Hold Time	t_{KXDX}	0.25	-	0.3	-	0.3	-	0.4	-	ns	2
Output Times											
Echo Clock High Pulse Width	t_{CHCL}	t_{KHKL}-0.1	t_{KHKL}+0.1	t_{KHKL}-0.1	t_{KHKL}+0.1	t_{KHKL}-0.2	t_{KHKL}+0.2	t_{KHKL}-0.3	t_{KHKL}+0.3	ns	2
Echo Clock Low Pulse Width	t_{CLCH}	t_{KLKH}-0.1	t_{KLKH}+0.1	t_{KLKH}-0.1	t_{KLKH}+0.1	t_{KLKH}-0.2	t_{KLKH}+0.2	t_{KLKH}-0.3	t_{KLKH}+0.3	ns	2
Clock Crossing to Echo Clock	t_{CXCH}	0.5	2.3	0.5	2.3	0.5	2.3	0.5	2.3	ns	3
Clock Crossing to Echo Clock Low	t_{CXCL}	0.5	2.3	0.5	2.3	0.5	2.3	0.5	2.3	ns	3
Echo Clock High to Output Vaild	t_{CHQV}	-0.20	0.20	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	
Echo Clock Low to Output Valid	t_{CLQV}	-0.20	0.20	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	
Echo Clock High to Output Hold	t_{CHQX}	-0.20		-0.20		-0.20		-0.20		ns	
Echo Clock Low to Output Hold	t_{CLQX}	-0.20		-0.20		-0.20		-0.20		ns	
Echo Clock High to Output High-Z	t_{CHQZ}		0.20		0.20		0.20		0.20	ns	
Echo Clock High to Output Low-Z	t_{CHLZ}	-0.20		-0.20		-0.20		-0.20		ns	
$\overline{G}$ Low to Output Valid	t_{GLQV}	-	1.7	-	1.8	-	1.9	-	2.1	ns	
$\overline{G}$ High to Output Low-Z	t_{GHQX}	0.5		0.5		0.5		0.5		ns	
$\overline{G}$ High to Output High-Z	t_{GHQHZ}	-	1.7	-	1.8	-	1.9	-	2.1	ns	

Notes: 1. The maximum cycle time must be limited to guarantee AC timing specification.
2. This parameter is guaranteed by design, and may not be tested at values shown in the table.
3. This parameter refers to CQ and $\overline{CQ}$ rising and falling edges.
4. K and $\overline{K}$ Clocks must be used differencitally to meet AC timing specifications.

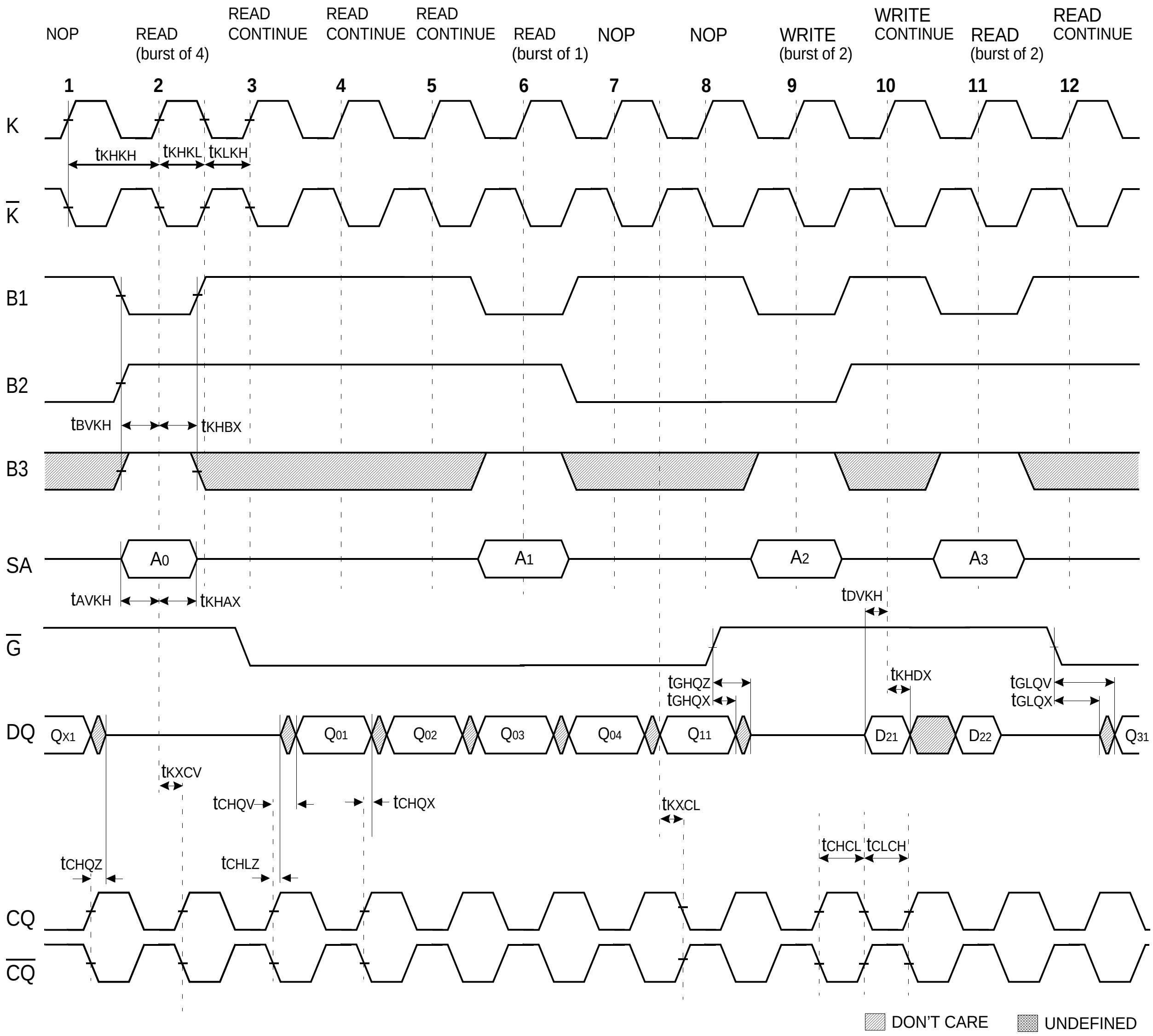
TIMING WAVEFORMS FOR DOUBLE DATA RATE CYCLES (Burst Length=4, 2)



NOTE

1. Q01 refers to output from address A. Q02 refers to output from the next internal burst address following A, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. Doing more than one Read Continue or Write Continue will cause the address to wrap around.

TIMING WAVEFORMS FOR SINGLE DATA RATE CYCLES
(Burst Length=4, 2, 1)

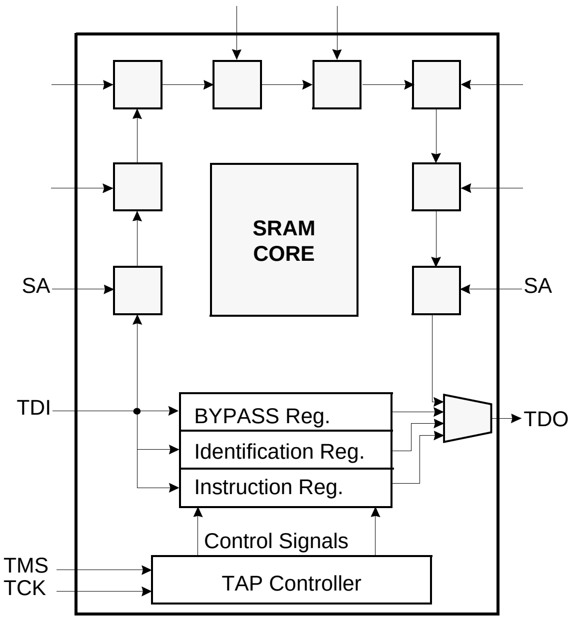


NOTE :
1. Q_{01} refers to output from address A_0. Q_{02} refers to output from the next internal burst address following A_0, etc.
2. Outputs are disabled(High-Z) one clock cycle after NOP detected or after no pending data requests are present.
3. This devices supports cycle lengths of 1, 2, 4. Continue(B1=HIGH, B2=HIGH, B3=X) up to three times following a B1 operation. Any further Continue assertions constitute invalid operations.
4. This device will have an address wraparound if further Continues are applied.

IEEE 1149.1 TEST ACCESS PORT AND BOUNDARY SCAN-JTAG

The SRAM provides a limited set of IEEE standard 1149.1 JTAG functions. This is to test the connectivity during manufacturing between SRAM, printed circuit board and other components. Internal data is not driven out of SRAM under JTAG control. In conformance with IEEE 1149.1, the SRAM contains a TAP controller, Instruction Register, Bypass Register and ID register. The TAP controller has a standard 16-state machine that resets internally upon power-up, therefore, TRST signal is not required. It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfacing with normal operation of the SRAM, TCK must be tied to V_{SS} to preclude mid level input. TMS and TDI are designed so an undriven input will produce a response identical to the application of a logic 1, and therefore can be left unconnected. But they may also be tied to V_{DD} through a resistor. TDO should be left unconnected.

JTAG Block Diagram

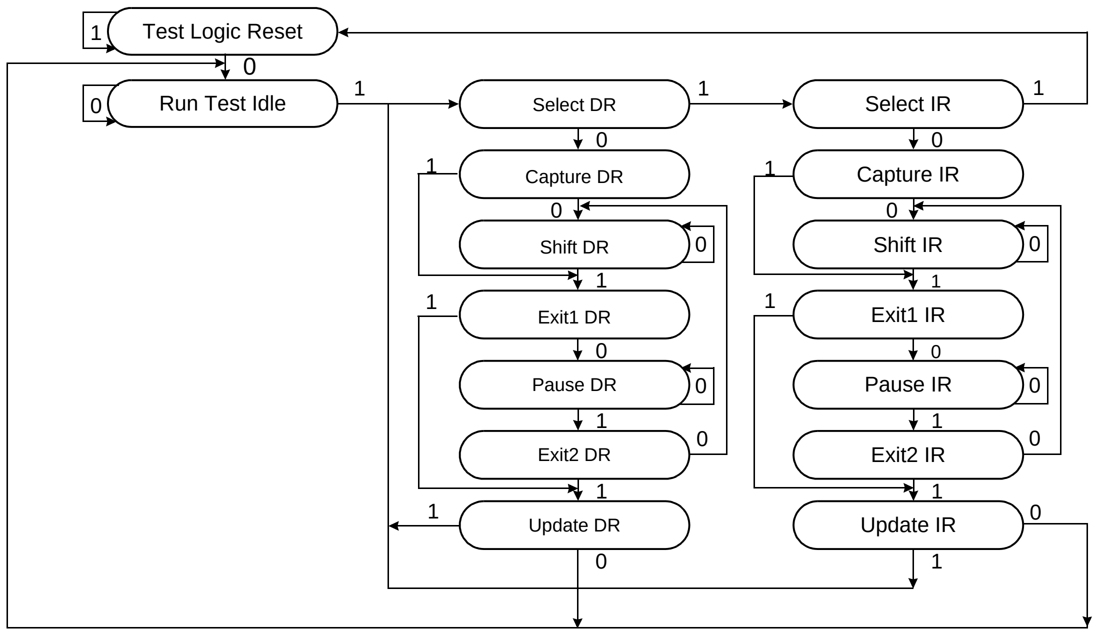


JTAG Instruction Coding

IR2	IR1	IR0	Instruction	TDO Output	Notes
0	0	0	EXTEST	Boundary Scan Register	1
0	0	1	IDCODE	Identification Register	2
0	1	0	SAMPLE-Z	Boundary Scan Register	1
0	1	1	BYPASS	Bypass Register	3
1	0	0	SAMPLE	Boundary Scan Register	4
1	0	1	BYPASS	Bypass Register	3
1	1	0	BYPASS	Bypass Register	3
1	1	1	BYPASS	Bypass Register	3

NOTE :
1. Places DQs in Hi-Z in order to sample all input data regardless of other SRAM inputs.
2. TDI is sampled as an input to the first ID register to allow for the serial shift of the external TDI data.
3. Bypass register is initiated to V_{SS} when BYPASS instruction is invoked.
   The Bypass Register also holds serially loaded TDI when exiting the Shift DR states.
4. SAMPLE instruction does not places DQs in Hi-Z.

TAP Controller State Diagram



SCAN REGISTER DEFINITION

Part	Instruction Register	Bypass Register	ID Register	Boundary Scan
1M x 18	3 bits	1 bits	32 bits	49 bits

ID REGISTER DEFINITION

Part	Revision Number (31:28)	Part Configuration (27:18)	Vendor Definition (17:12)	Samsung JEDEC Code (11: 1)	Start Bit (0)
1M x 18	0000	01000 00011	XXXXXX	00001001110	1

BOUNDARY SCAN EXIT ORDER(x18)

26	4A	SA		SA	6A	25
27	4C	SA		SA	6C	24
28	3A	SA		SA	7A	23
29	3B	SA		SA	7B	22
30	3C	SA		SA	7C	21
31	3D	SA		SA	7D	20
32	2B	DQ				
				DQ	9B	19
				DQ	8D	18
				DQ	7F	17
33	1D	DQ				
34	2F	CQ				
				DQ	9F	16
35	3H	DQ				
				DQ	8H	15
36	1H	DQ				
37	5A	ZQ		$\overline{G}$	5C	14
38	5B	B_1		K	5G	13
39	5K	B_2		$\overline{K}$	5H	12
40	5L	B_3		MODE	6L	11
41	4L	$\overline{LBO}$		DQ	9K	10
42	2K	DQ		DQ	7K	9
43	1M	DQ		$\overline{CQ}$	8M	8
				DQ	9P	7
44	3M	DQ				
45	2P	DQ				
46	1T	DQ		DQ	8T	6
				SA	7P	5
47	3P	SA		SA	7T	4
48	3T	SA		SA	6R	3
49	4R	SA		SA	5T	2
				SA	5R	1

* Reserved for Mode Pin

JTAG DC OPERATING CONDITIONS

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Supply Voltage	V_{DD}	1.7	1.8	1.9	V	
Input High Level	V_{IH}	1.5	-	V_{DD}+0.3	V	
Input Low Level	V_{IL}	-0.3	-	0.7	V	
Output High Voltage(I_{OH}=-2mA)	V_{OH}	1.5	-	V_{DD}	V	
Output Low Voltage(I_{OL}=2mA)	V_{OL}	V_{SS}	-	0.2	V	

NOTE : 1. The input level of SRAM pin is to follow the SRAM DC specification.

JTAG AC TEST CONDITIONS

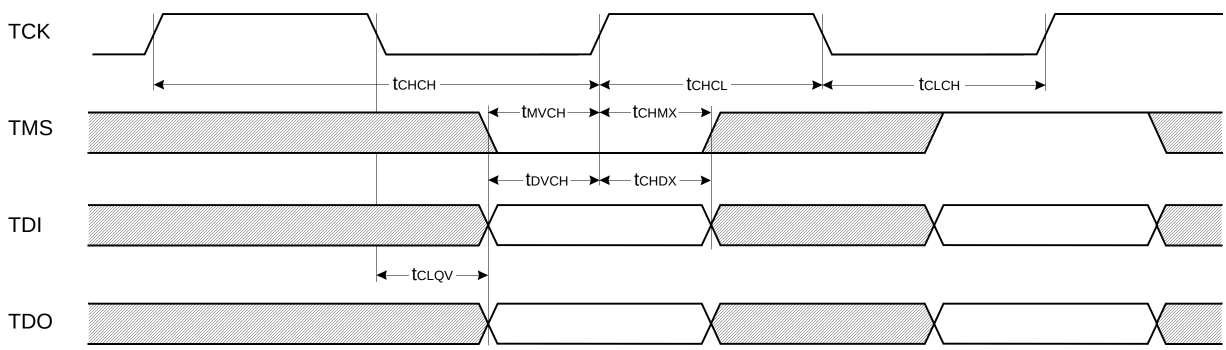
Parameter	Symbol	Min	Unit	Note
Input High/Low Level	V_{IH}/V_{IL}	1.8/0.0	V	
Input Rise/Fall Time	TR/TF	1.0/1.0	ns	
Input and Output Timing Reference Level		0.9	V	1

NOTE : 1. See SRAM AC test output load on page 5.

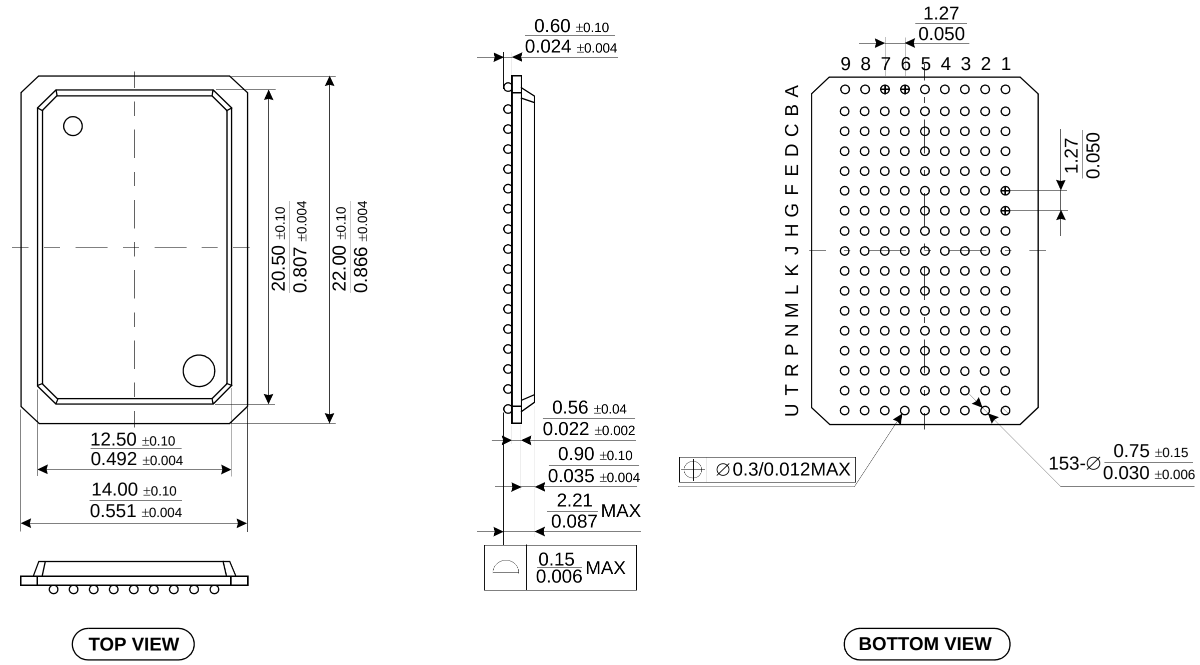
JTAG AC Characteristics

Parameter	Symbol	Min	Max	Unit	Note
TCK Cycle Time	t_{CHCH}	50	-	ns	
TCK High Pulse Width	t_{CHCL}	20	-	ns	
TCK Low Pulse Width	t_{CLCH}	20	-	ns	
TMS Input Setup Time	t_{MVCH}	5	-	ns	
TMS Input Hold Time	t_{CHMX}	5	-	ns	
TDI Input Setup Time	t_{DVCH}	5	-	ns	
TDI Input Hold Time	t_{CHDX}	5	-	ns	
Clock Low to Output Valid	t_{CLQV}	0	10	ns	

JTAG TIMING DIAGRAM



153 BGA PACKAGE DIMENSIONS



NOTE :
1. All Dimensions are in Millimeters.
2. Solder Ball to PCS Offset : 0.10 MAX.
3. PCB to Cavity Offset : 0.10 MAX.

153 BGA PACKAGE THERMAL CHARACTERISTICS

Parameter	Symbol	Thermal Resistance	Unit	Note
Junction to Ambient(at still air)	Theta_JA	TBD	°C/W	
Junction to Case	Theta_JC	TBD	°C/W	
Junction to Board	Theta_JB	TBD	°C/W	

NOTE : 1. Junction temperature can be calculated by : $T_J = T_A + P_D$ x Theta_JA.